

**ASSIGNMENT 4**

[Design of a combinational logic circuit using 2 input NAND gates for

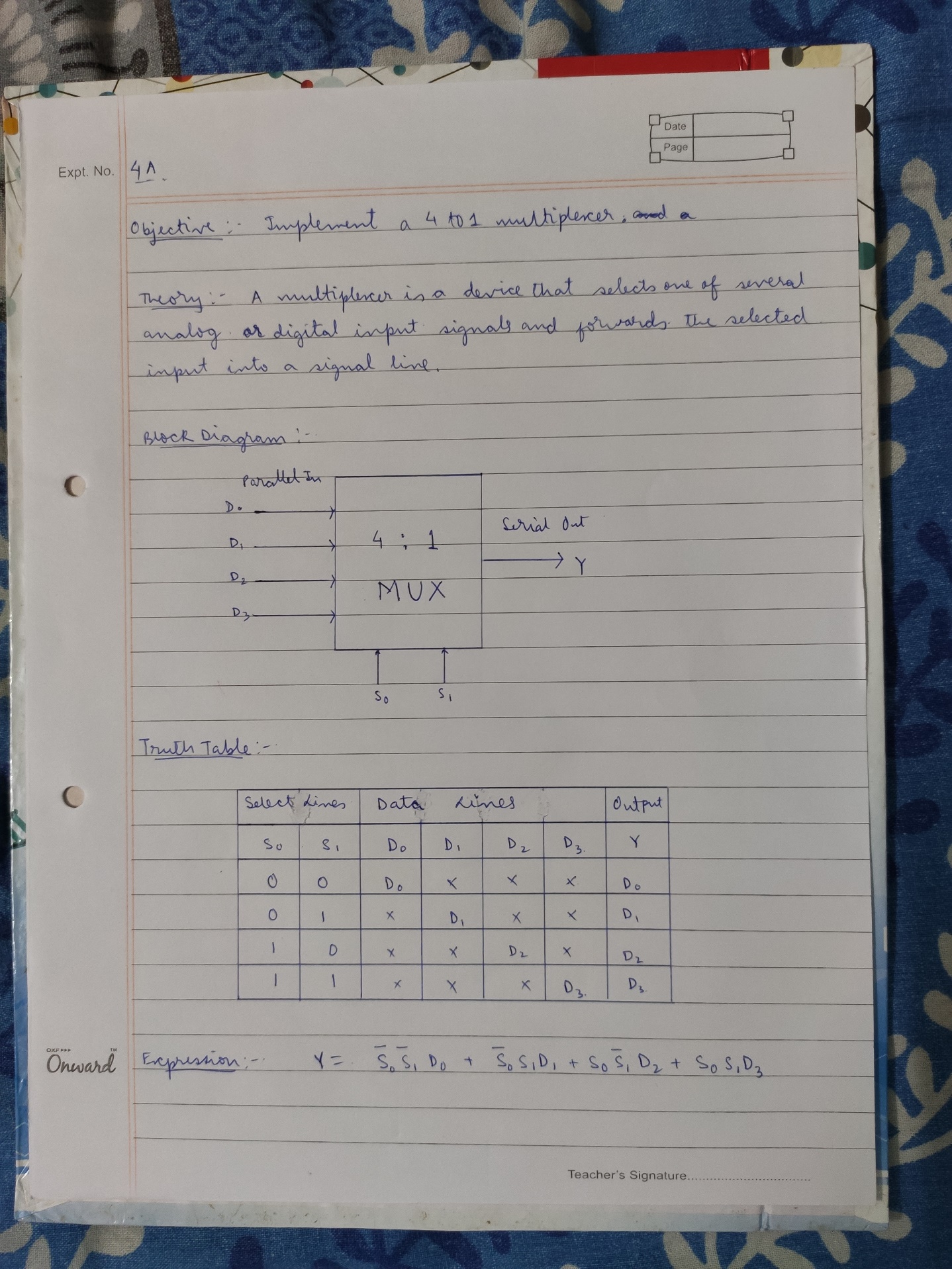
1. **4X1 MULTIPLEXER**
2. **1X4 DEMULTIPLEXER**]

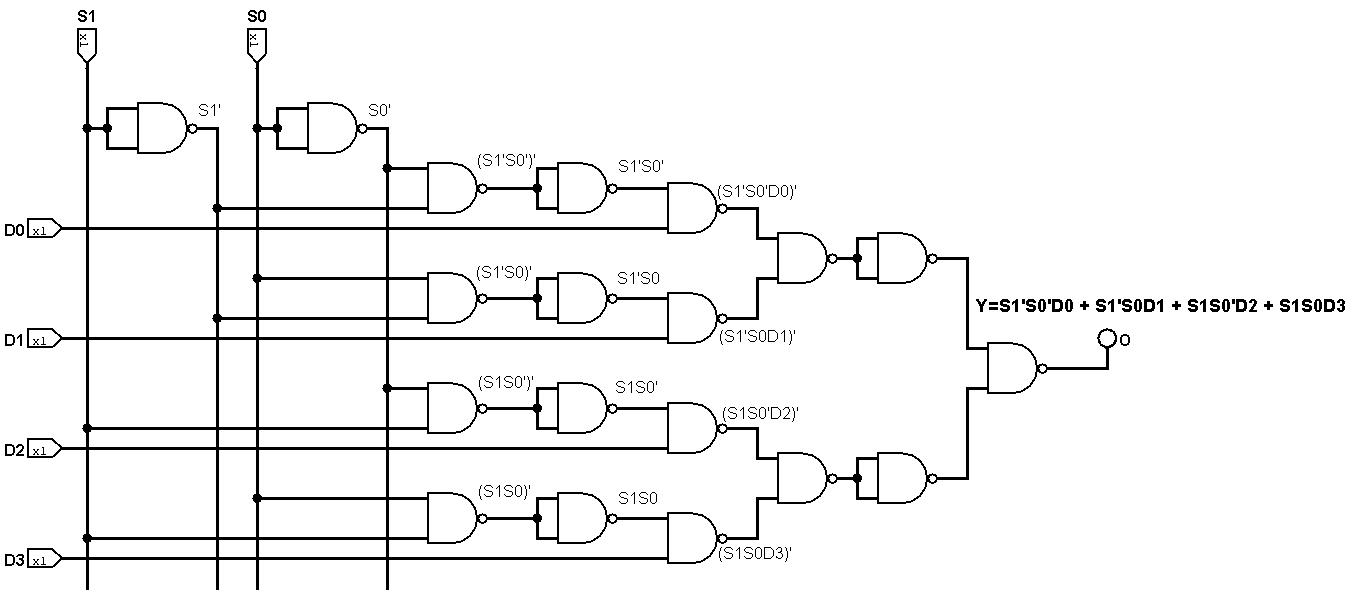


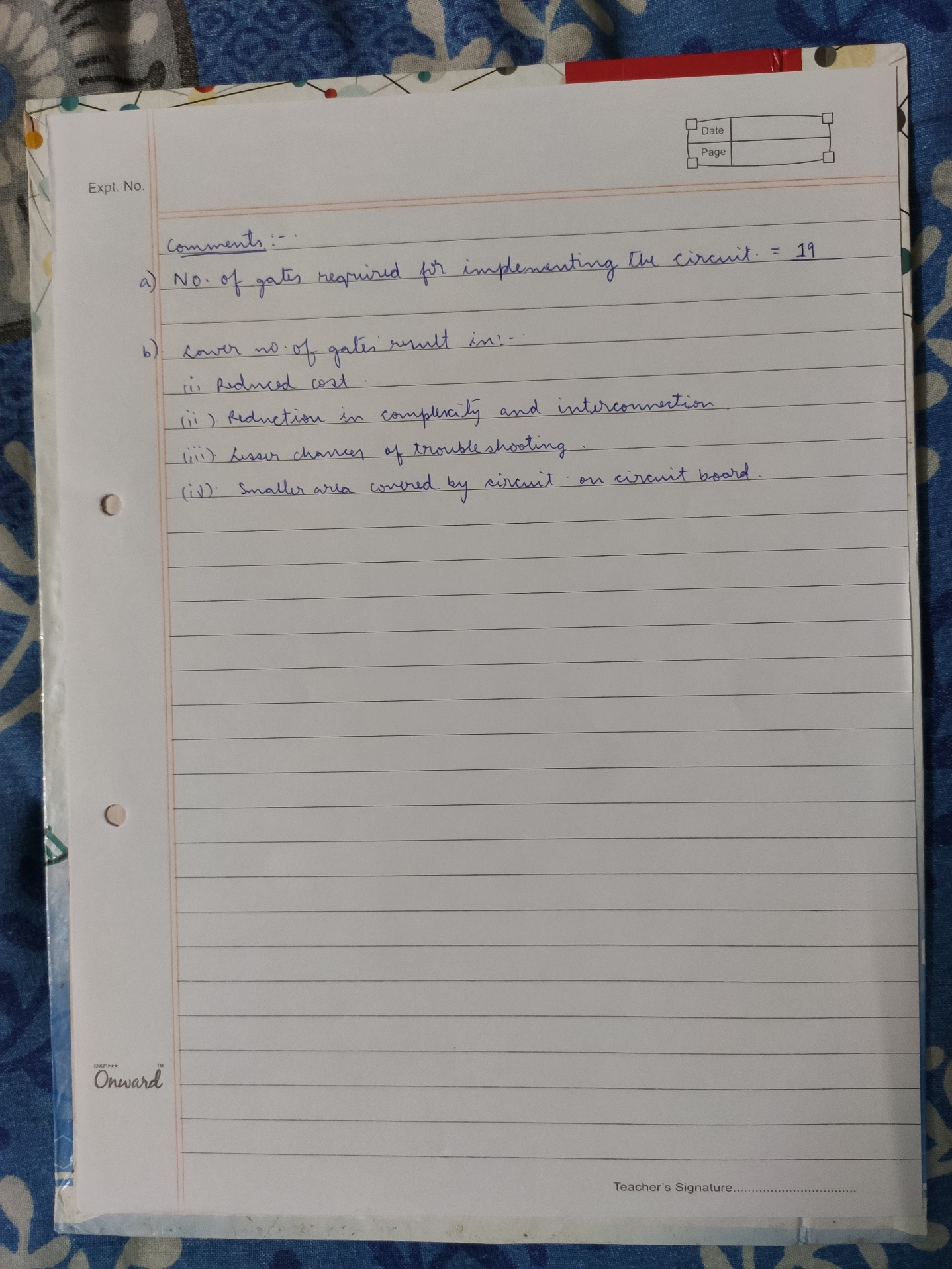
**NAME: ROHIT SADHU**

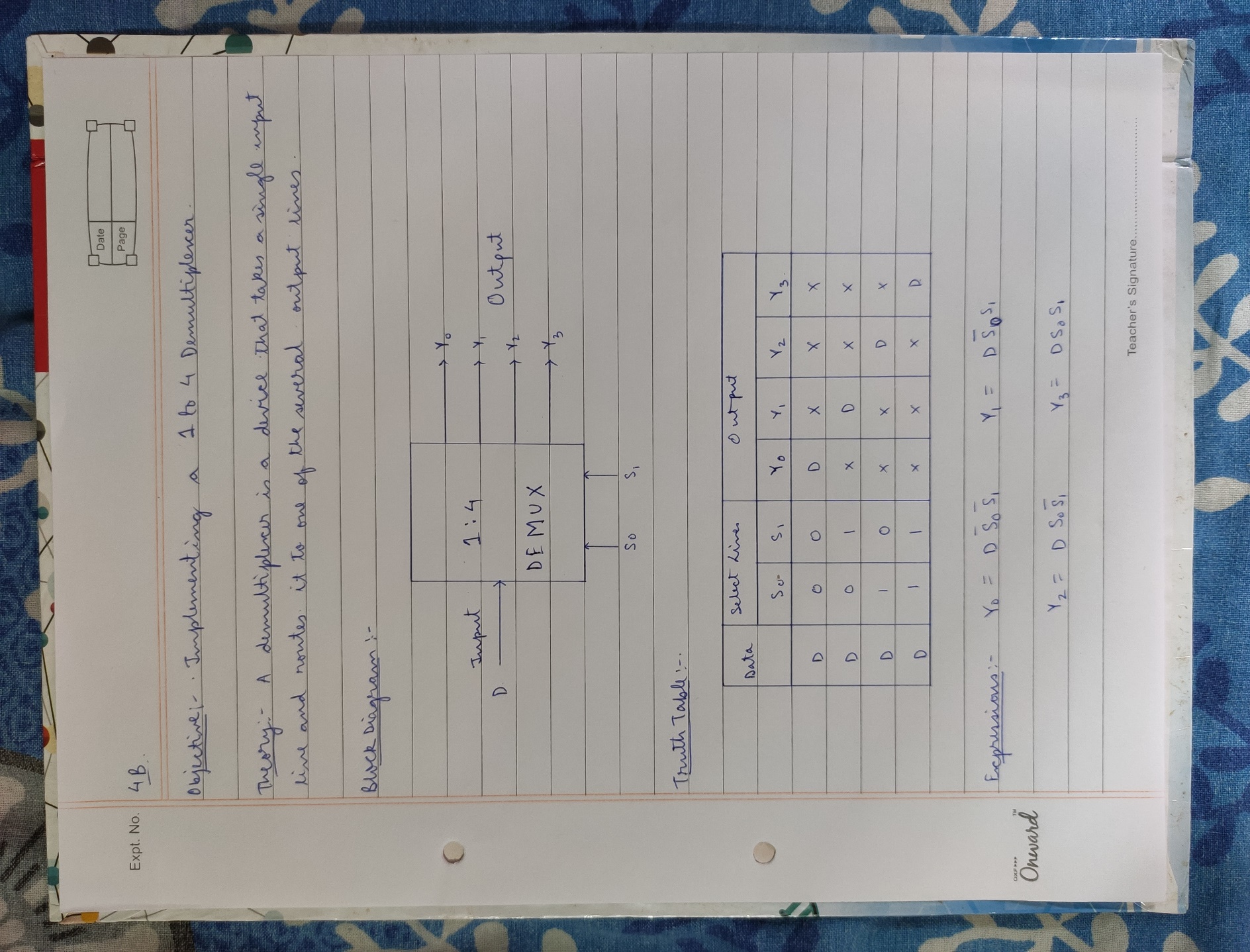
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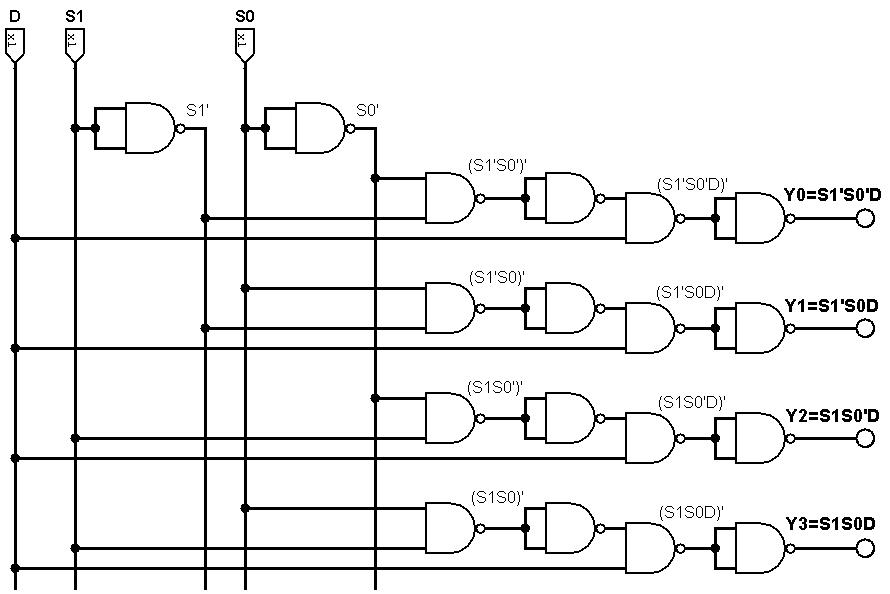




**CIRCUIT DIAGRAM: -**





**CIRCUIT DIAGRAM: -**

